

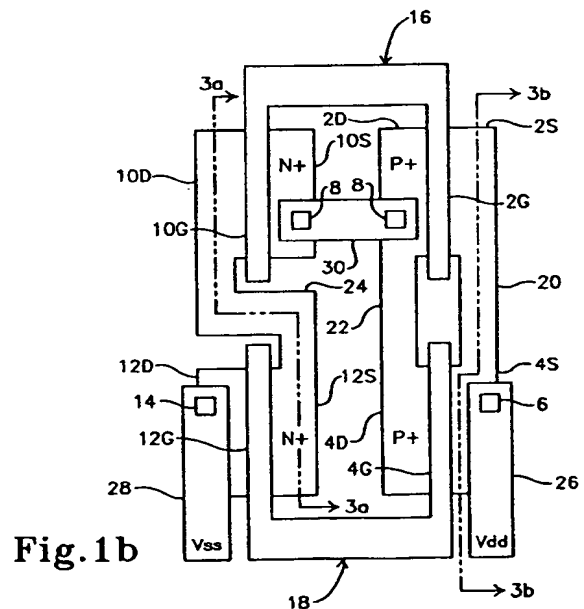


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Fig.1a



EP 0 585 601 A1

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to the prevention of reverse engineering of integrated circuits (ICs), and more particularly to security techniques in which interconnections between circuit elements are made undetectable.

Description of the Related Art

Several techniques have been used to reverse engineer ICs. Electron (e)-beam probing with a scanning electron microscope (SEM), either through SEM photographs or voltage contrast analysis, is the standard reverse engineering mechanism, although secondary ion mass spectrometry (SIMS), spreading resistance analysis and various other techniques have also been used. A general description of e-beam probing is provided in Lee, "Engineering a Device for Electron-beam Probing", IEEE Design & Test of Computers, 1989, pages 36-49.

Numerous ways to frustrate unwanted attempts to reverse engineer an IC have also been developed. For example, in Patent No. 4,766,516 to Ozdemir et al. (assigned to Hughes Aircraft Company, the assignee of the present invention), additional circuit elements that do not contribute toward the desired circuit function are added to an IC, and disguised with the visible appearance of being an ordinary part of the IC. The elements have physical modifications that are not readily visible but cause them to function in a different manner, inhibiting the proper functioning of the IC in case of an attempted copying or other unauthorized use. When the apparent function rather than the actual function of the disguised elements are copied, the resulting circuit will not operate properly.

In Patent No. 4,583,011 to Pechar a pseudo-MOS (metal oxide semiconductor) device is given a depletion implant that is not readily visible to a copier, who would infer from the device's location in the circuit that it would be enhancement-mode. A somewhat related approach is taken in French patent publication no. 2 486 717 by Bassett et al., published January 15, 1982; the circuit doping is controlled so that some devices which appear to be transistors actually function as either open or short circuits. And in Patent No. 4,603,381 to Gutttag the memory of a central processing unit is programmed by the doping of its channel regions, rather than by the presence or absence of gates, to protect permanently programmed software.

Instead of disguising circuit elements, some systems have a mechanism to protect the circuit from operating until a correct access code has

been entered. Such systems are described in Patent Nos. 4,139,864 to Schulman and 4,267,578 to Vetter.

Each of the above protection schemes requires additional processing and/or uses additional circuitry that is dedicated to security and does not contribute to the basic functioning of the circuit. This increases the cost of circuit production and complicates the circuitry.

SUMMARY OF THE INVENTION

The present invention seeks to provide a security system and method to protect against IC reverse engineering that is very difficult to detect, can be implemented without any additional fabrication steps and is compatible with computer added design (CAD) systems that allow many different kinds of logic circuits to be constructed with ease.

A logic gate is formed in a semiconductor substrate in accordance with the invention by forming doped regions in the substrate of like conductivity, and interconnecting at least some of the like conductivity regions by similarly doping interconnect portions of the substrate that run between such regions. The interconnects and the regions they connect are preferably doped simultaneously through a common dopant implantation mask to similar dopant concentrations, resulting in an integral structure for the doped regions and their interconnects. Metallized interconnects are provided as needed between p- and n- doped regions, and metallic microbridges can be used to span strips of polycrystalline gate material that interrupt an interconnect circuit. A metallized interconnect can also be formed above the substrate to further mask a doped interconnect from observation.

Although doped implants are generally not as highly conductive as metallized interconnects, their resistance is low enough to serve an interconnect function at very large scale integration (VLSI) dimensions. Because the implanted connections are not visible to SEM or optical viewing technique, the purpose or function of the logic gates cannot be deduced, thus making the circuit very difficult to reverse engineer. Many different circuit designs that use the security technique can be stored in a CAD library and readily recalled for use as desired.

Further features and advantages of the invention will be apparent to those skilled in the art from the following detailed description, taken together with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGs. 1a and 1b are respectively a schematic diagram and a plan view of a NAND gate in accordance with the invention;

FIGs. 2a and 2b are respectively a schematic diagram and a plan view of a NOR gate in accordance with the invention;

FIGs. 3a and 3b are sectional views taken along section lines 3a-3a and 3b-3b of FIG. 1b that illustrate the simultaneous formation of transistor source/drain regions and implanted interconnects therebetween with a common implant process and common masks for n-channel and p-channel transistors, respectively;

FIG. 4 is a sectional view taken along section line 404 in FIG. 2b of interconnected source/drain regions in accordance with the invention, with the implanted interconnect shaded by an upper metallization layer;

FIG. 5 is a simplified plan view of a logic gate that uses metallized microbridges to span polycrystalline gate layers in accordance with the invention; and

FIG. 6 is a sectional view of a microbridge span.

DETAILED DESCRIPTION OF THE INVENTION

An important aspect of this invention is that it does not rely upon any modifications or additions to the functioning of the circuitry that is to be protected from reverse engineering, nor does it require any additional processing steps or equipment. Instead, a highly effective deterrent to reverse engineering is accomplished in a streamlined manner that adds neither cost, time nor complexity to the basic circuitry.

Implementations of the invention in the form of NAND and NOR gates will first be described. Using such gates as building blocks, many different types of logic circuitry can be designed. A distinct advantage of the invention is that different types of logic circuits may be made to look alike, thus confusing a potential reverse engineer.

FIG. 1a is a schematic diagram of a conventional two-input NAND gate circuit, with a pair of p-channel transistors 2, 4 connected in parallel between a positive voltage terminal 6 and an output terminal 8, and a pair of n-channel transistors 10, 12 connected in series between a negative voltage terminal 14 and the output terminal 8. Input terminals 16 and 18 for the inputs designated A and B are connected to respective p-channel/n-channel transistor pairs.

An implementation of this basic logic gate in accordance with the invention is shown in FIG. 1b. The sources, drains and gates of each of the transistors are indicated by the same transistor numbers as in FIG. 1, followed by S, D or G, respectively. The transistor sources and drains (the designation of an element as a source or drain is somewhat arbitrary) are fabricated in a conventional manner by implanting dopant ions into the

circuit substrate. The p+ sources and drains of the p-channel devices 2 and 4 are typically doped with a boron ion implant at a density of about 4×10^{15} ion/cm², and an implantation energy of about 30 keV. The n+ source and drain regions of the n-channel transistors 10 and 12 are typically doped in accordance with industry standards with arsenic ions at a density of about 5×10^{15} /cm², and an implant energy of about 150 keV. Either a masked ion flood beam or a focused ion beam may be used; doping by older gaseous diffusion techniques may also be employed.

Rather than connecting the transistor regions of like conductivity with metallized interconnects in the conventional fashion, such connections are made by means of doping implants into the substrate between the desired sources and drains. Three such interconnections 20, 22 and 24 are shown between sources 2S and 4S, drains 2D and 4D and drain 10D-source 12S, respectively. The implant interconnections are preferably established simultaneously with the source and drain implants by providing appropriate openings in the implantation mask (if flood beam implantation is employed), or by extending the scanning area of a focused ion beam. As an alternate to implantation a conventional gaseous diffusion process could be employed to establish the doping, but this is less preferable than implantation. By using the same source/drain fabrication step to also fabricate the implanted interconnections, the interconnections have the same dopant concentration as the sources and drains and are formed integrally therewith.

The remainder of the gate circuit is fabricated in a conventional manner. The polysilicon gates (assuming a silicon substrate is used) can be formed either before or after the source and drain and interconnect implants, while metallized connectors 26, 28 and 30 are run over intervening insulating layers to provide external connections to the Vdd terminal 6, Vss terminal 14 and output terminal 8.

FIG. 2a is a schematic diagram of a conventional NOR gate, while FIG. 2b illustrates its implementation in accordance with the invention. It uses the same transistor layout as the NAND gate of FIGs. 1a and 1b, but the implanted interconnects between the transistors of like conductivity is reversed. Specifically, p-channel transistors 2 and 4 are connected in series between positive voltage terminal 6 and output terminal 8 by a p-doped implant 32 that runs between drain 4D of transistor 4 and source 2S of transistor 2; the n-channel transistors 10 and 12 are connected in parallel between negative voltage terminal 14 and output terminal 8 by n-doped implant interconnects 34 and 36 between the sources and gates of transistors 10 and 12, respectively.

FIGS. 3a and 3b are sectional views taken along the section lines 3a-3a and 3b-3b of FIG. 1b, respectively, illustrating the fabrication of the source, drain and interconnection implants, but excluding the polysilicon and metallization layers. The devices are formed in a semiconductor substrate 38 that for illustrative purposes is silicon, but may also be GaAs or some other desired semiconductor material. The circuit fabrication can be accomplished with a conventional process, such as that described in Frederiksen, *Intuitive CMOS Electronics*, McGraw-Hill Publishing Co., 1989, pages 134-145; it is a distinct advantage of the invention that it does not require any special processing to implement.

In a typical CMOS process, a protective oxide layer about 250 Angstroms thick is first laid down over the semiconductor substrate 38. A well is then implanted through openings in the oxide layer for each FET whose source and drain is of the same conductivity type as the substrate doping. With substrate 38 illustrated as having an n- doping, a somewhat more heavily doped p-well 40 would be implanted about 3 microns deep for the n-channel devices (FIG. 3a). The wells are then subjected to a long, high temperature anneal, typically at about 1,150° C for about 10 hours.

The next step is the FET source and drain implants. For the n-channel devices an oxide mask 42 is laid down over the substrate with openings at the desired locations for the sources and drains of the n-channel devices. In the case of two n-channel FETs 10 and 12 that are to be interconnected by means of a ion implantation in accordance with the invention, a single continuous mask opening 44 is provided for the drain 10D of FET 10, the source 12S of FET 12, and the interconnection implant 24 that runs between them. The implantation is then formed, preferably with a flood beam indicated by numeral 46, of suitable n-dopant ions such as arsenic.

As in conventional processing, a separate implant mask 48 is provided for the p-channel devices (FIG. 3b). A single continuous opening 50 is provided in the mask for each interconnection implant and the transistor elements which they connect; these are illustrated as p-channel FET sources 2S and 4S and interconnect implant 20. Implantation is preferably performed with a flood beam, indicated by numeral 52, of a suitable p-type dopant such as boron.

The implantation can be performed exactly the same as in prior unsecured processes, the only difference being that the implant is now done through a larger opening in each mask that includes the implanted interconnection as well as the FET sources and drains. No differences in processing time or techniques are required, and the oper-

ator need not even know that the mask provides for circuit security. The circuits are then completed in a conventional manner, with threshold implants made into the FET channels to set the transistor characteristics. A field oxide is laid down as usual, but it also defines active areas which encompass "actual" as well as "possible" interconnect regions. Otherwise, the interconnect paths would be apparent. Polysilicon is then deposited and doped either by diffusion or ion implantation to form the channels and the interconnects. A dielectric is then deposited and metallization layers added to establish inputs, outputs and bias signals. Finally an overglass coating is laid down over the entire chip.

The implant interconnections have been demonstrated to be virtually invisible to SEM scanning in a secondary electron mode. They are also believed to be invisible to a voltage contrast SEM analysis. However, to guard against the possibility of their being detected through voltage contrast, the upper metallization can be designed to mask the implants. Thus, voltage contrast analysis of the interconnect implantations cannot be performed until the upper metallization layers are stripped away to expose the implants, but if the upper metallization is removed the voltage contrast analysis cannot be performed because there is no longer a mechanism for applying a voltage to the implant; the metallization that must be removed to expose the implants provided this function. Such a structure is illustrated in FIG. 4, which shows a sectional view of FET drains 10D and 12D and their interconnect implant 36 from FIG. 2b, after the circuit fabrication has been completed. The structure employs a p-well process; a corresponding structure would result from an n-well process. A field oxide layer 54 insulates the FETs from adjacent devices, while the contact 14 to FET drain 12D is made from metallization layer 28 through an opening in an oxide insulating layer 56. Several metallization layers separated by oxide layers are normally provided, although for simplicity only one metallization layer 28 is illustrated. This layer 28 is topped by a final oxide layer 58, and then a thicker overglass coating 60 of SiO₂ that extends over the entire chip and is lightly doped so as to prevent the buildup of a static charge.

While the implanted interconnections described thus far can successfully connect different FETs, having them pass under strips of polysilicon that extend along the substrate surface should be avoided. This is because the polysilicon is biased to function as a gate, and when crossing over an implanted interconnection would in effect establish a transistor at that location. To avoid this, metal microbridges can be used to span polysilicon strips. Microbridges are known elements that are described, for example, in U.S. Patent Nos.

4,239,312 and 4,275,410, assigned to Hughes Aircraft Company.

FIG. 5 illustrates a three-input NAND gate that uses this approach; metallized connectors that are added at a later stage in the fabrication are not shown. The gate includes three p-channel FETs 62a, 62b and 62c, and three n-channel FETs 64a, 64b and 64c. Common polysilicon gate strips 66a, 66b and 66c are provided for transistor pairs 62a, 64a; 62b, 64b; and 62c, 64c, respectively. The polysilicon strips extend over the substrate surface between their respective FETs, as well as over the FET channels. To connect the upper FETs 62a-62c in parallel, their drains are electrically tied together by an interconnecting implant 60 in accordance with the invention. However, a corresponding interconnection cannot be made between their sources, since it would have to cross the polysilicon gate strip 66b and 66c. To overcome this, the FET sources are extended by implant interconnects to locations adjacent to the polysilicon strips 66b and 66c, and these extensions are then interconnected by means of microbridges 68b and 68c that span strips 66b and 66c, respectively. An additional microbridge 68a is shown spanning polysilicon strip 66a between the FET 62a source extension and an island 70 that is implanted into the substrate along with the FET sources, drains and interconnects. This bridge can either serve a dummy purpose to confuse a reverse engineer, or island 70 can provide a contact point to receive a signal from an upper metallization for transmission to the sources of FETs 62a-62c.

The lower FETs 64a-64c can be connected in series directly with implanted interconnects 72a and 72b between the source of FET 64a and the drain of FET 64b, and the source of 64b and drain of 64c, since there are no polysilicon strips in the paths of these connections. However, an implanted source extension of FET 64c is shown connected to an implant island 74a above the drain of FET 64a via a series of implanted islands 74b and 74c and microbridges 76a, 76b and 76c that span polysilicon strips 64a, 64b and 64c, respectively. These microbridges can also either serve a dummy purpose, or be used to transmit a signal between a metallized connection to island 74a and the drain of FET 64c.

FIG. 6 is a simplified sectional view of microbridge 68a and its interconnection with the circuitry. One leg of the microbridge contacts the upper surface of p-doped implant island 70, while the opposite leg contacts the p-doped implant interconnection between FETs 62a and 62b. The center portion of the microbridge spans the polysilicon strip 66a, with an insulating dielectric 78 between the two elements.

By replacing metal interconnects with implanted interconnections that are not visible to SEM or optical viewing techniques, the purpose or function of the protected circuits cannot be deduced by a reverse engineer. Furthermore, it will be difficult for the reverse engineer to determine when the circuits are covertly connected by etching all metal, oxide and nitride layers deposited later in the fabrication process, because with the dimensions employed for modern VLSI circuits normal drying, ion milling, ion spectroscopy and SIMS techniques do not have the required sensitivity.

The secure NAND and NOR gates described herein and other types of logic gates can form the building blocks for many complicated logic sequences, which would therefore be virtually impossible to reverse engineer. Although a spreading resistance reverse engineering analysis might still theoretically be possible, with a small probe measuring the circuit's resistivity over a very small volume and stepped progressively across the surface, in practice this would also not work. The upper layers would have to be stripped away to analyze the implanted interconnects with the spreading resistance technique, but in so doing the positional registration of the implanted areas with respect to the stripped metallization would be lost. Furthermore, spreading resistance analysis is a mechanical process that is much slower than SEM analysis. The reverse engineer would still be able to see the transistors, but not the connections between them.

Since the only required change in the fabrication process is for a modification in the openings of the ion implantation masks, a new set of standard masks with the modified openings could be provided and used as standard elements of the circuit design process. This makes the invention particular suitable to CAD systems, with the designer simply selecting a desired secured logic gate design from a library of such gates.

While several illustrative embodiments of the invention have been shown and described, numerous variations and alternate embodiments will occur to those skilled in the art. Such variations and alternate embodiments are contemplated, and can be made without departing from the spirit and scope of the invention as defined in the appended claims.

Claims

1. A secure integrated circuit (IC), comprising:
 - a semiconductor substrate (38),
 - a plurality of doped IC elements (2, 4, 10, 12; 62, 64) formed in said substrate (38), and
 - an interconnect (20, 22, 24; 32, 34, 36; 60, 70, 72, 74) for at least one of said elements (2,

4, 10, 12; 62, 64),

characterized in that said interconnect (20, 22, 24; 32, 34, 36; 60, 70, 72, 74) comprises a dopant implant (20, 22, 24; 32, 34, 36; 60, 70, 72, 74) in said substrate (38) of like conductivity to said element (2, 4, 10, 12; 62, 64), and provides an electrical signal path to interconnect said element (2, 4, 10, 12; 62, 64) with another portion of the IC.

2. The circuit of claim 1, characterized in that at least one element (2, 4, 10, 12; 62, 64) and said interconnect (20, 22, 24; 32, 34, 36; 60, 70, 72, 74) have similar dopant concentrations.
3. A secure integrated circuit (IC) logic circuit, comprising:
 - a semiconductor substrate (38), and
 - a logic gate formed in said substrate with doped regions (2S, 4S; 2D, 4D; 10D, 12S; 2S, 4D; 10S, 12S; 10D, 12D; 62a, 62b, 62c; 64a, 64b, 64c) of like conductivity, and a doped interconnect (20, 22, 24; 32, 34, 36; 60, 70, 72, 74) implant in said substrate (38) of like conductivity to said doped regions (2S, 4S; 2D, 4D; 10D, 12S; 2S, 4D; 10S, 12S; 10D, 12D; 62a, 62b, 62c; 64a, 64b, 64c) and electrically interconnecting said regions (2S, 4S; 2D, 4D; 10D, 12S; 2S, 4D; 10S, 12S; 10D, 12D; 62a, 62b, 62c; 64a, 64b, 64c).
4. The circuit of claim 3, characterized in that said doped regions (2S, 4S; 2D, 4D; 10D, 12S; 2S, 4D; 10S, 12S; 10D, 12D; 62a, 62b, 62c; 64a, 64b, 64c) and interconnect implant (20, 22, 24; 32, 34, 36; 60, 70, 72, 74) have similar dopant concentrations.
5. The circuit of claim 4, characterized in that the doping of said doped regions (2S, 4S; 2D, 4D; 10D, 12S; 2S, 4D; 10S, 12S; 10D, 12D; 62a, 62b, 62c; 64a, 64b, 64c) are integral with the doping of said interconnect implant (20, 22, 24; 32, 34, 36; 60, 70, 72, 74).
6. The circuit of any of claims 3-5, characterized in that said logic gate has p- (2S, 4S; 2D, 4D; 62a, 62b, 62c) and n-doped (10D, 12D; 10S, 12S; 64a, 64b, 64c) regions, with a p-doped interconnection implant (20, 22, 60) interconnecting p-doped regions (2S, 4S; 2D, 4D; 62a, 62b, 62c), an n-doped interconnection implant (24, 72) interconnecting n-doped regions (10D, 12D; 10S, 12S; 64a, 64b, 64c), and a metallization connector (30) interconnecting p- and n-doped regions (2S, 4S; 2D, 4D; 10D, 12S; 2S, 4D; 10S, 12S; 10D, 12D; 62a, 62b, 62c; 64a, 64b, 64c).
7. The circuit of claim 6, characterized in that said logic gate comprises a complementary metal oxide semiconductor (CMOS) gate.
8. The circuit of any of claims 3-7, characterized in that said logic gate comprises a NAND gate with a pair of n-doped metal oxide semiconductor field effect transistors (MOSFETs) (10, 12, 64) connected in series by an n-doped interconnect (24, 72) between a first voltage reference (Vss) and an output (8), a pair of p-doped MOSFETs (2, 4, 62) connected in parallel by a p-doped interconnect (20, 22, 60) between a second voltage reference (Vdd) and said output (8), metallized connectors (28, 26) for said first and second voltage references (Vss, Vdd), and a metallized output connector (30).
9. The circuit of any of claims 3-7, characterized in that said logic gate comprises a NOR gate with a pair of p-doped metal oxide semiconductor field effect transistors (MOSFETs) (2, 4) connected in series by a p-doped interconnect (32) between a first voltage reference (Vdd) and an output (8), a pair of n-doped MOSFETs (10, 12) connected in parallel by an n-doped interconnect (34, 36) between a second voltage reference (Vss) and said output (8), metallized connectors (26, 28) for said first and second voltage references (Vss, Vdd), and a metallized output connector (30).
10. The circuit of any of claims 1-9, characterized in that it further comprises a metallization (28) above said substrate (38) masking said interconnect (20, 22, 24; 32, 34, 36; 60, 70, 72, 74) from external observation.
11. The circuit of any of claims 1-10, characterized in that said logic gate includes a pair of said doped interconnects (70, 74a, 74b, 74c) of like conductivity separated by a strip of polycrystalline substrate material (66a, 66b, 66c) on said substrate (38), and a metallic micro bridge (68a, 68b, 68c; 76a, 76b, 76c) spanning said strip of polycrystalline material (66a, 66b, 66c) and connecting said doped interconnects (70, 74a, 74b, 74c).
12. A method of fabricating an integrated circuit (IC), comprising:
 - forming IC elements in a semiconductor substrate (38) with doped regions (2S, 4S; 2D, 4D; 10D, 12S; 2S, 4D; 10S, 12S; 10D, 12D; 62a, 62b, 62c; 64a, 64b, 64c) that have like conductivity, and
 - interconnecting at least some of said like

conductivity doped regions (2S, 4S; 2D, 4D; 10D, 12S; 2S, 4D; 10S, 12S; 10D, 12D; 62a, 62b, 62c; 64a, 64b, 64c) by doping interconnect portions (20, 22, 24; 32, 34, 36; 60, 70, 72, 74) of said substrate (38) between said regions (2S, 4S; 2D, 4D; 10D, 12S; 2S, 4D; 10S, 12S; 10D, 12D; 62a, 62b, 62c; 64a, 64b, 64c) to a like conductivity with said regions (2S, 4S; 2D, 4D; 10D, 12S; 2S, 4D; 10S, 12S; 10D, 12D; 62a, 62b, 62c; 64a, 64b, 64c).

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13. The method of claim 12, characterized in that said interconnect portions (20, 22, 24; 32, 34, 36; 60, 70, 72, 74) of said substrate (38) are doped to a similar dopant concentration as the dopant concentrations of the regions (2S, 4S; 2D, 4D; 10D, 12S; 2S, 4D; 10S, 12S; 10D, 12D; 62a, 62b, 62c; 64a, 64b, 64c) they interconnect.

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14. The method of claim 12 or 13, characterized in that said interconnect portions (20, 22, 24; 32, 34, 36; 60, 70, 72, 74) are formed integrally with the doped regions (2S, 4S; 2D, 4D; 10D, 12S; 2S, 4D; 10S, 12S; 10D, 12D; 62a, 62b, 62c; 64a, 64b, 64c) they interconnect.

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15. The method of any of claims 12-14, characterized in that said interconnect portions (20, 22, 24; 32, 34, 36; 60, 70, 72, 74) and the regions (2S, 4S; 2D, 4D; 10D, 12S; 2S, 4D; 10S, 12S; 10D, 12D; 62a, 62b, 62c; 64a, 64b, 64c) they interconnect are doped simultaneously.

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16. The method of any of claims 12-15, characterized in that said interconnect portions (20, 22, 24; 32, 34, 36; 60, 70, 72, 74) and the regions (2S, 4S; 2D, 4D; 10D, 12S; 2S, 4D; 10S, 12S; 10D, 12D; 62a, 62b, 62c; 64a, 64b, 64c) they interconnect are doped through a common dopant implantation mask (42, 48).

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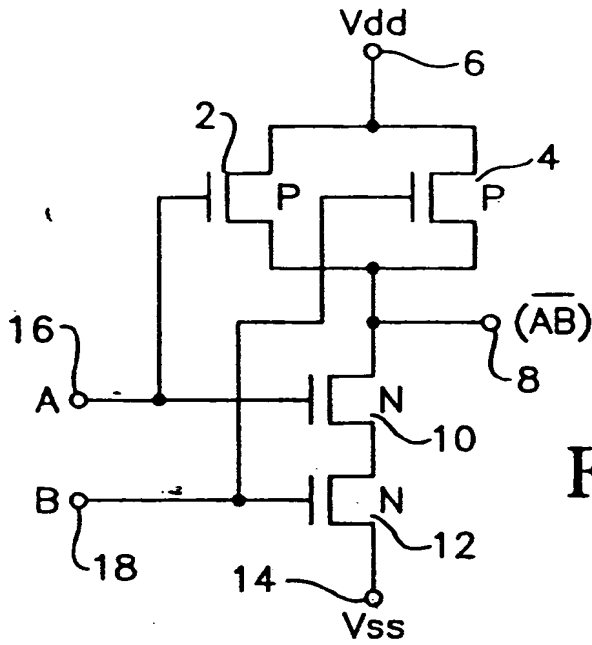


Fig. 1a

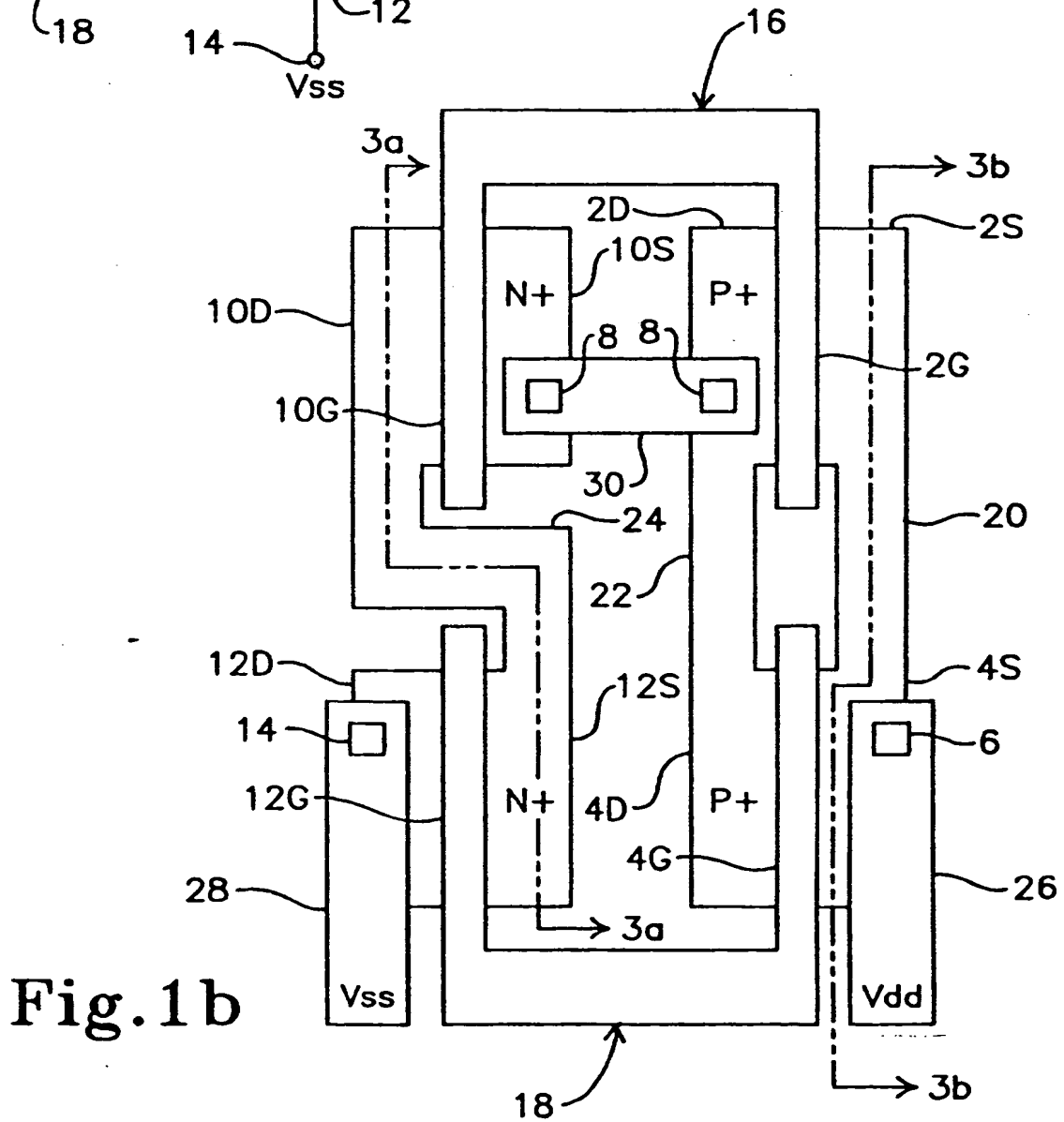


Fig. 1b

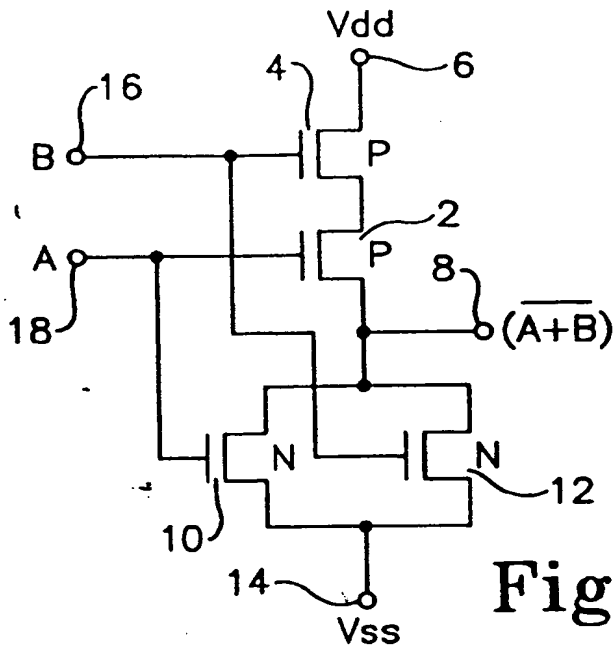


Fig. 2a

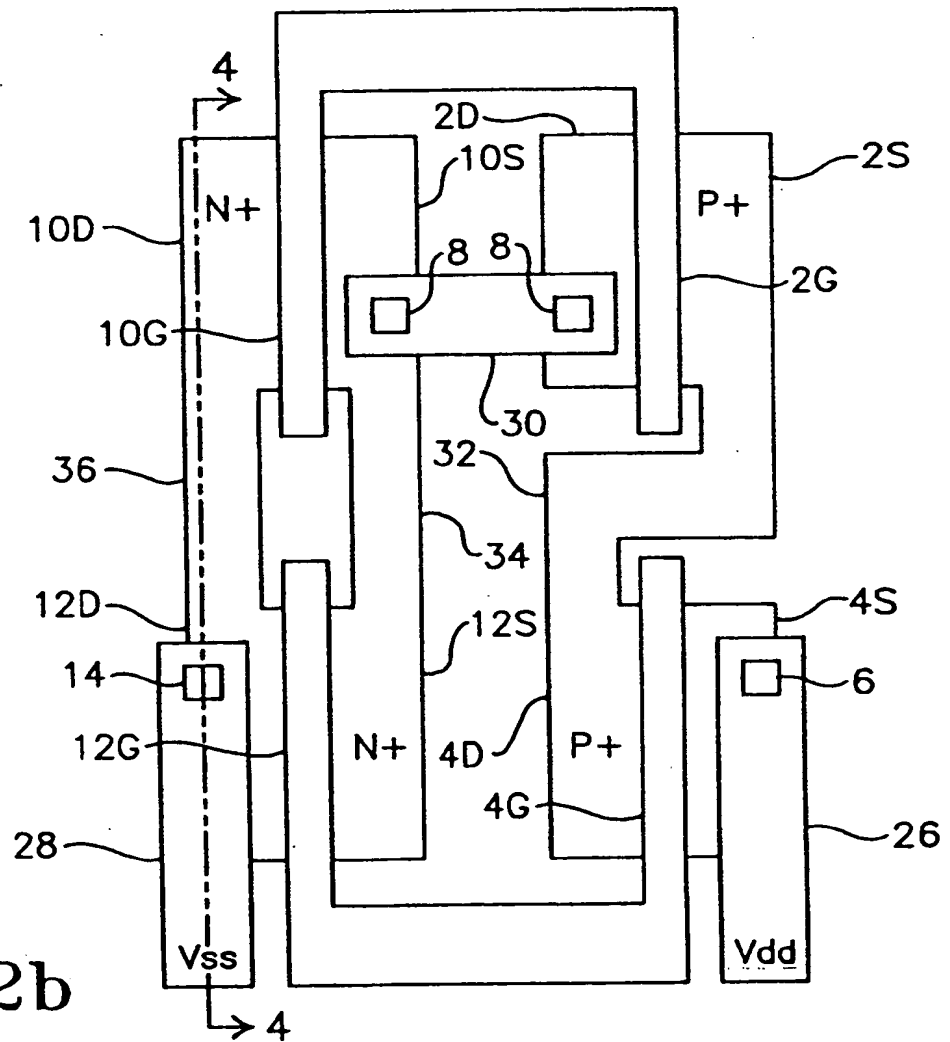


Fig. 2b

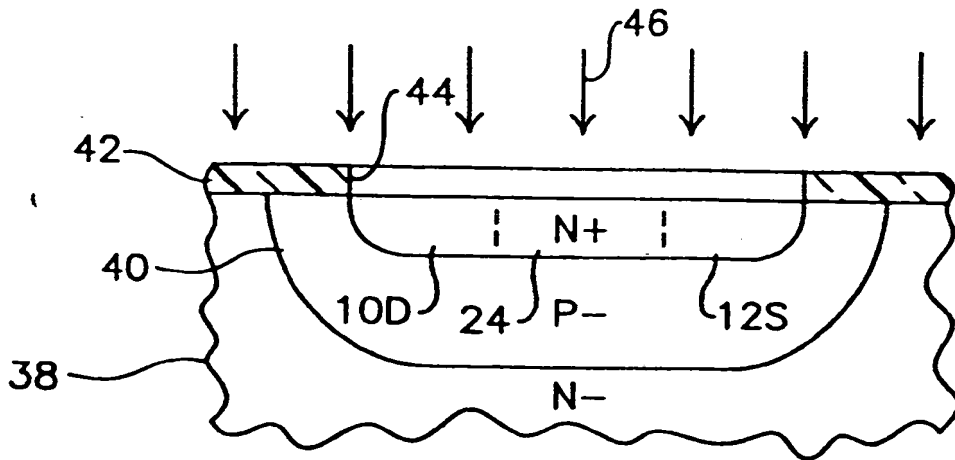


Fig.3a

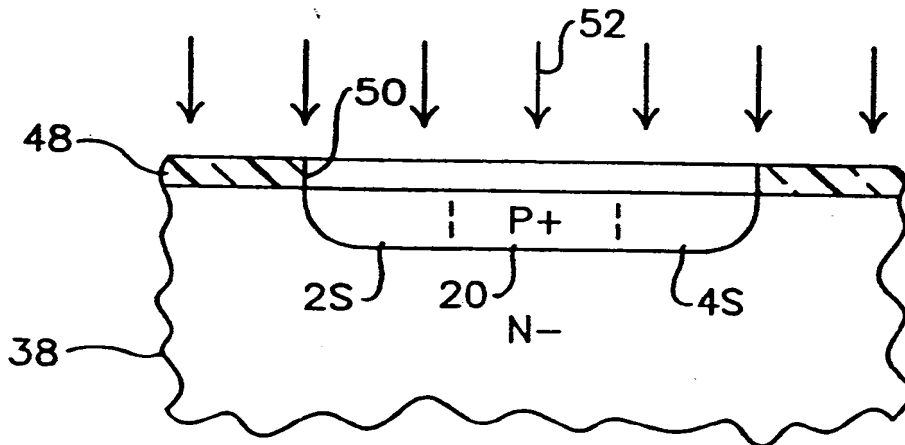


Fig.3b

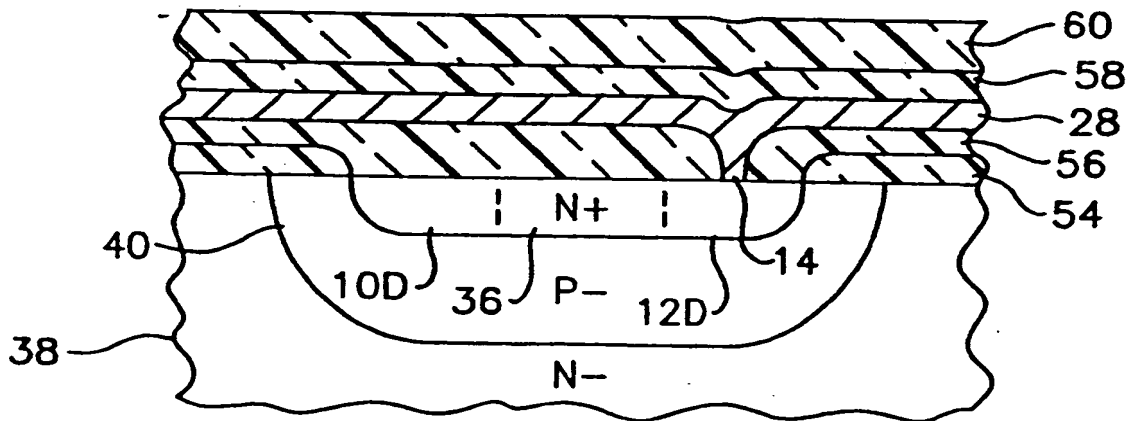
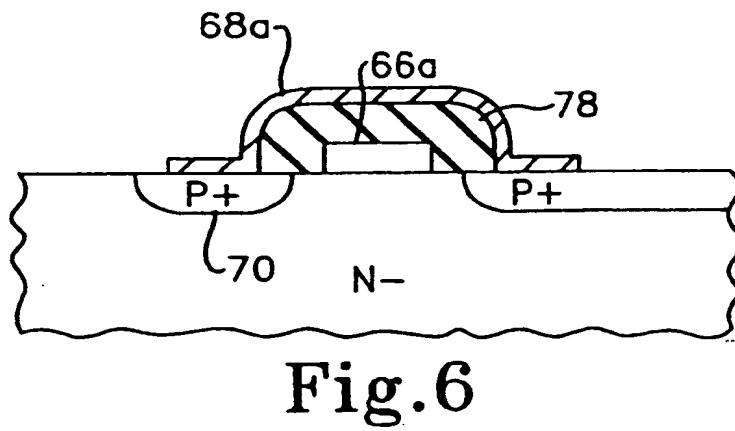
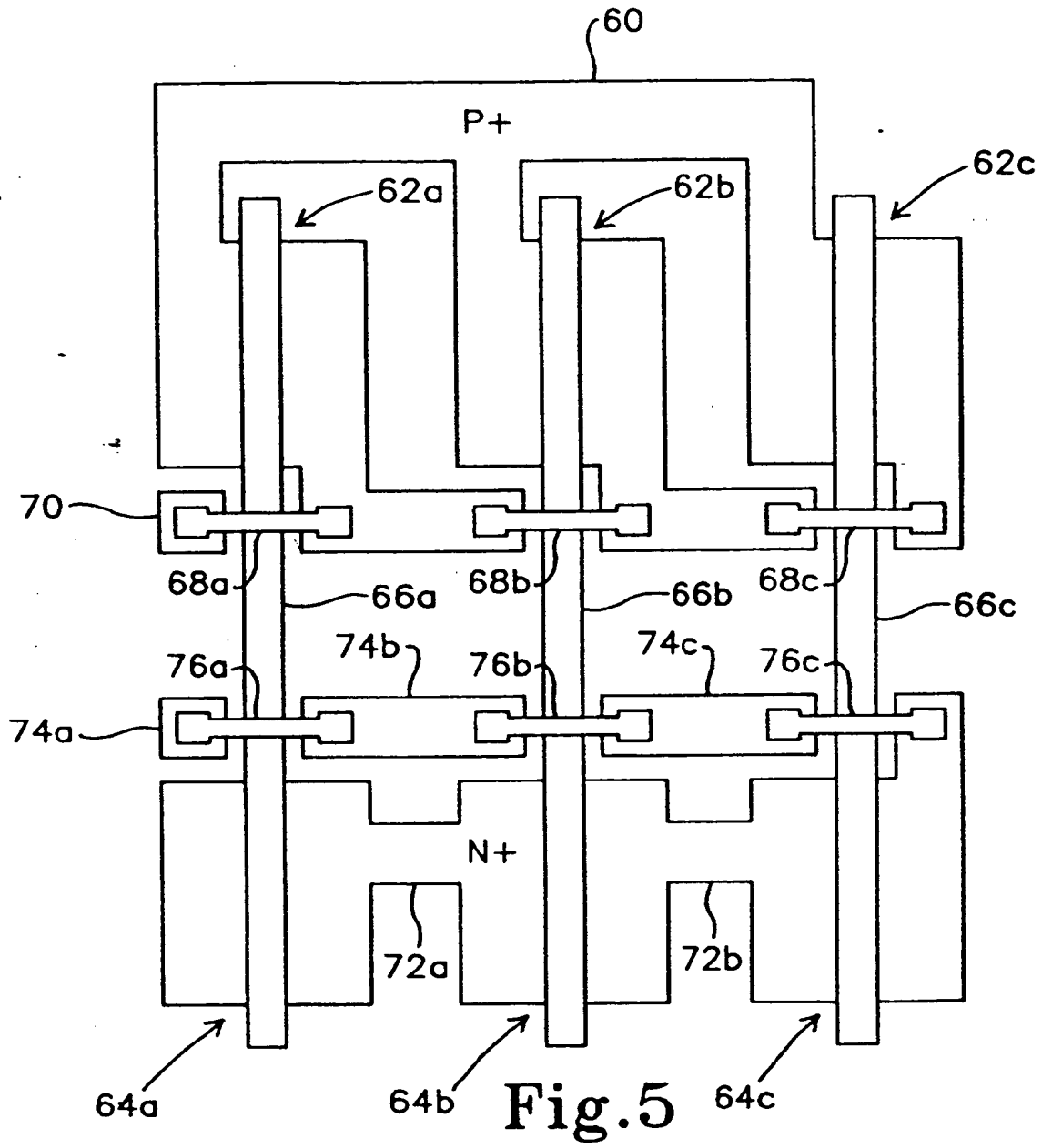


Fig.4





European Patent
Office

EUROPEAN SEARCH REPORT

Application Number

EP 93-11 1978

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	PATENT ABSTRACTS OF JAPAN vol. 016, no. 197 (P-1350) 12 May 1992 & JP-A-40 28 092 (TOSHIBA CORP.) * abstract *	1-8	H01L23/58 H01L27/02
P, X	& US-A-5 138 197 (K. KUWANA) * column 1, line 11 - column 2, line 23; figures 6-8 *	1-8	
X	US-A-4 291 391 (P. K. CHATTERJEE ET ALL) * column 2, line 14 - column 3, line 23; figures 1-3 *	1,2, 12-15	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			H01L
The present search report has been drawn up for all claims			
Place of search BERLIN		Date of completion of the search 29 NOVEMBER 1993	Examiner ROUSSEL A.T.
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

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